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10EC/TE71

Seventh Semester B.E. Degree Examination, June/July 2017
Computer Communication Networks

Time: 3 hrs.   Max. Marks:100

Note: *Answer FIVE full questions, selecting*
at least TWO questions from each part.

PART – A

1   a.   Explain the ISO-OSI reference model with a neat diagram. Discuss the function of each layer. **(10 Marks)**
    b.   Explain the signaling system seven (SS7) protocol with a neat diagram. **(05 Marks)**
    c.   Match the following functions to the appropriate layers in the OSI model:
         i)   Interface to the transmission media.
         ii) Dividing the transmitted bit stream into frames
         iii) Route determination
         iv) Reliable process to process message delivery
         v)   Format and code conversion services **(05 Marks)**

2   a.   Explain the bit stuffing and unstuffing by taking a suitable example. **(05 Marks)**
    b.   Explain the configuration modes of HDLC protocol with neat diagrams. **(05 Marks)**
    c.   Explain the stop and wait protocol with neat diagram. **(10 Marks)**

3   a.   Explain the procedure for pure aloha protocol with a neat diagram. **(06 Marks)**
    b.   A slotted aloha network transmits 200 bit frames using a shared channel of 200 kbps bandwidth. Find the throughput, if the system produces,
         i)   1000 frames per second
         ii) 500 frames per second
         iii) 250 frames per second **(06 Marks)**
    c.   Explain the working of CSMA/CD with a neat diagram. **(08 Marks)**

4   a.   Compare the data rates for standard Ethernet, fast Ethernet, gigabit Ethernet and ten gigabit Ethernet. **(04 Marks)**
    b.   Identify whether the following Mac addresses are unicast, multicast or broad cast.
         i)   4A : 30 : 10 : 21 : 10 : 1A
         ii) 47 : 20 : 1B : 2E : 08 : EE
         iii) FF : FF : FF : FF : FF : FF **(06 Marks)**
    c.   What are the common standard Ethernet implementation? Explain with neat diagrams. **(10 Marks)**

PART – B

5   a.   Explain each of the following in brief:
         i)   Passive hub
         ii) Repeater
         iii) Bridge
         iv) Router
         v)   Gateway **(10 Marks)**
    b.   Explain each of the following in brief :
         i)   Bus backbone networks
         ii) Star backbone networks **(06 Marks)**
    c.   What is vlan? Explain. **(04 Marks)**

6 a. Explain the IPV4 datagram format with a neat diagram. **(10 Marks)**

   b. Explain the classful addressing schemes. **(06 Marks)**

   c. A block of addresses is granted to an organization. If the IP address of one of the host is 205.16.37.39/28, find the first address and last address in the block. **(04 Marks)**

7 a. What is the difference between a direct delivery and indirect delivery? **(04 Marks)**

   b. What is multicasting? Explain with a neat diagram and mention the applications of multicasting. **(08 Marks)**

   c. Classify the four types of links defined by OSPF and explain. **(08 Marks)**

8 a. Explain the TCP segment format with a neat diagram. **(10 Marks)**

   b. What are the three domains of the domain name space? Explain. **(06 Marks)**

   c. How does recursive resolution differ from the iterative resolution? **(04 Marks)**

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Seventh Semester B.E. Degree Examination, June/July 2017

Optical Fiber Communication

Time: 3 hrs.   Max. Marks:100

Note: *Answer FIVE full questions, selecting*
at least TWO questions from each part.

PART – A

1. a. Summarize the inherent advantages of optical fiber over conventional copper cables. **(06 Marks)**

   b. Describe with neat diagram different types of optical fiber waveguides. Using ray theory, explain the propagation of light inside the fiber. **(08 Marks)**

   c. A silica optical fiber with a core diameter large enough to be considered by ray theory analysis has a core refractive index of 1.5. A light ray is incidented at the core-cladding interface with a critical angle of 78.5°. Estimate:
   i) Refractive index of cladding
   ii) Numerical aperture
   iii) The acceptance angle in air for the fiber **(06 Marks)**

2. a. Illustrate the different types of scattering losses in optical fiber with suitable equations. **(08 Marks)**

   b. Explain what is meant by the critical bending radius for an optical fiber. Write equation of critical radius of curvature for multimode and single mode fibers. **(06 Marks)**

   c. A multimode fiber with a core refractive index of 1.5, a relative refractive index difference of 3% and an operating wavelength of 0.82 μm. Estimate the critical radius of curvature at which large bending losses occur. **(06 Marks)**

3. a. Draw and explain the cross-sectional view of a typical AℓGaAs double heterojunction LED, along with the energy diagram. **(08 Marks)**

   b. Sketch and explain the GaAs homojunction injection laser with a Fabry-Perot cavity. **(06 Marks)**

   c. A planar LED is fabricated from Gallium Arsenide which has a refractive index of 3.6,
   i) Calculate the optical power emitted into air as a percentage of the internal optical power for the device when the transmission factor at the crystal-air interface is 0.68.
   ii) When the optical power generated internally is 50% of the electric power, determine the external power efficiency. **(06 Marks)**

4. a. With the aid of simple sketches, outline optical fiber coupler types and their functions. **(08 Marks)**

   b. Discuss different types of fiber misalignment and the factors which causes the losses due to those misalignment. **(06 Marks)**

   c. A single mode fiber has the following parameters:
        Normalised frequency (V) = 2.40
        Core refractive index (n_1) = 1.46
        Core diameter (2a) = 8μm
        Numerical aperture (NA) = 0.1
        Normalised spot size (ω) = 3.12 μm.
   Estimate the total insertion loss of a fiber joint with a lateral misalignment (Y) of 1 μm and an angular misalignment (θ) of 1°. **(06 Marks)**

PART – B

5   a. Briefly explain the quantum limit. **(04 Marks)**
    b. What is a Burst_Mode receiver? Explain. **(06 Marks)**
    c. Derive the equation for performance fidelity of an analog receiver. Substantiate that for a large optical signals, signal to noise ratio represents the quantum limit for receiver sensitivity. **(10 Marks)**

6   a. With a diagram, briefly explain the operation of multichannel amplitude modulation. **(08 Marks)**
    b. Explain the radio frequency over fiber concept of a broadband wireless access network for interconnecting antenna base stations with the central controlling office. **(08 Marks)**
    c. In a multimode link using LED as optical source, material dispersion related rise time degradation is 21 ns over the 6 km link. Receiver has a 25 MHz bandwidth. Fiber has 500 MHz.km bandwidth-distance product with mode mixing parameter, q = 0.7. Assuming LED with drive circuit has rise time of 15 ns, modal-dispersion-induced fiber rise time is 3.9 ns and the contribution to the rise-time degradation from the receiver is 14 ns. Calculate link rise time. **(04 Marks)**

7   a. Describe the operational principles of WDM, depicting the implementation of a typical WDM network containing various types of optical amplifier. **(08 Marks)**
    b. With a neat diagram, explain the working principle of Mach-Zehnder inter-ferometer multiplexer. **(08 Marks)**
    c. The input wavelengths of a 2 × 2 silicon Mach-Zehnder inter ferometer are separated by 10 GHz. The effective refractive index in the waveguide is 1.5. Calculate waveguide length difference. **(04 Marks)**

8   a. Explain with the aid of neat diagram, three possible EDFA configurations. **(06 Marks)**
    b. Describe:
       i) SONET/SDH frame format
       ii) SONET/SDH rings **(10 Marks)**
    c. An EDFA is pumped at 980 nm with a 30 mW pump power. If the gain at 1550 nm is 20 dB, calculate maximum input power. **(04 Marks)**

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Time: 3 hrs.   Max. Marks:100

Note: *Answer FIVE full questions, selecting*
at least TWO questions from each part.

PART – A

1   a.   Draw the control characteristics of SCR, GTO and MCT with circuit diagrams and waveforms of control signal and output voltage.   **(09 Marks)**
    b.   What is Schottky diode? Mention its advantages.   **(04 Marks)**
    c.   What are the peripheral effects of power electronic equipment and mention remedies of its.   **(07 Marks)**

2   a.   Explain the following parameters with respect to switching limits:
        (i)   Second breakdown (SB).
        (ii)   Forward –biased safe operating area.
        (iii)   Power derating.
        (iv)   Breakdown voltages.   **(12 Marks)**
    b.   Explain proportional and antisaturation control of a base drive.   **(08 Marks)**

3   a.   For the circuit shown in Fig. Q3 (a) obtain the minimum gate pulse width is required for reliable triggering of the SCR if gated at $\frac{\pi}{3}$ angle in every +ve half cycle. Assume $V_s = 325\sin 314t$ and latching current of 15 mA.   **(06 Marks)**
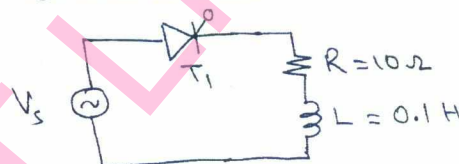

Fig. Q3 (a)

    b.   Explain the operation of a full wave RC-firing circuit with waveforms.   **(08 Marks)**
    c.   Explain how thyristors are protected against high $\frac{di}{dt}$.   **(06 Marks)**

4   a.   For the circuit shown in Fig. Q4 (a), find the average load voltage and current if the load resistance is 10 Ω and firing angle is 45°. Assume supply of 230 V, 50 Hz.   **(06 Marks)**

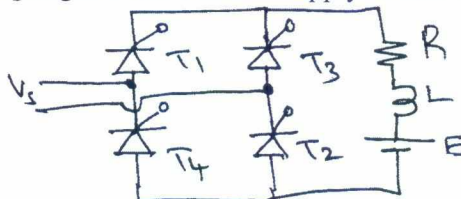Fig. Q4 (a)

    b.   Explain the operation of single phase semiconverter with circuit and waveforms. Derive the expression for the average and rms value of the output voltage. (Assume RL-load).   **(10 Marks)**
    c.   What are the advantages of circulating current mode dual converter?   **(04 Marks)**

PART – B

5 a. Explain the operation of a self commutation by resonating load and also derive the expression of $i(t) = V_s \sqrt{\dfrac{C}{L}} \sin\left(\dfrac{1}{\sqrt{LC}} t\right)$. **(12 Marks)**

    b. For the circuit shown in Fig. Q5 (b) the current through R_1 and R_2 is 25 A and turn off time of both SCR's is 40 μsec. Find the value of capacitor for successful commutation. **(04 Marks)**
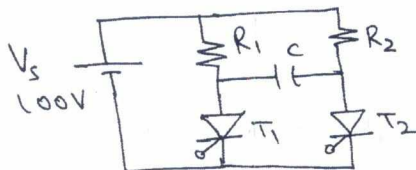

Fig. Q5 (b)

    c. Compare natural and forced commutation. **(04 Marks)**

6 a. Explain the operation of a single phase Bi-directional controller with resistive load. Derive the expression of RMS value of the output voltage. **(10 Marks)**

    b. A single phase AC voltage controller shown in Fig. Q6 (b) has a resistive load of 10 Ω and input voltage of 120 V, 60 Hz. The delay angle of thyristor T_1 is $\dfrac{\pi}{2}$. Determine

        (i)   RMS value of the output voltage.
        (ii)   Input power factor.
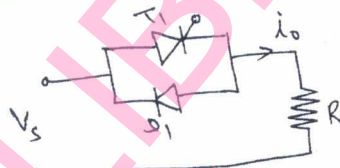   (iii)   Average input current. **(07 Marks)**

Fig. Q6 (b)

    c. Mention the applications of AC voltage controllers. **(03 Marks)**

7 a. Explain the working principles of step down chopper with RL-load. Derive the expression of peak-peak ripple in the load current. **(14 Marks)**

    b. A step up chopper has input voltage of 220 V and output voltage of 660 V. If the non-conducting time of thyristor chopper is 100 μsec. Compute the pulse width of the output voltage. (conduction period). **(06 Marks)**

8 a. Explain the following performance parameters of a inverters:
        (i)   Harmonic factor of nth harmonic.
        (ii)   Total harmonic distortion.
        (iii)   Distortion factor. **(06 Marks)**

    b. Explain the operation of single phase bridge inverters. **(10 Marks)**

    c. What is inverter? Mention applications of it. **(04 Marks)**

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Seventh Semester B.E. Degree Examination, June/July 2017
Embedded System Design

Time: 3 hrs.   Max. Marks:100

Note: *Answer FIVE full questions, selecting*
at least TWO questions from each part.

PART – A

1   a. What is an embedded system? Explain briefly the various components in a microprocessor based embedded system with a block diagram.   **(10 Marks)**
    b. What are the considerations and important steps in developing an embedded system? Briefly describe the major elements of the embedded system development life cycle.   **(10 Marks)**

2   a. Explain the block diagram of a special purpose microprocessor.   **(06 Marks)**
    b. Compare:
        (i)   Harvard and Von-Neumann architecture.
        (ii)   Big Endian and Little Endian formats.
        (iii) RISC and CISC registers.   **(06 Marks)**
    c. Write the block diagram of RTN for a microprocessor Datapath and memory interface. Also explain instruction cycle steps with ISA level instructions.   **(08 Marks)**

3   a. Write the inside and outside diagrams for SRAM along with read and write operations.   **(08 Marks)**
    b. Explain an associative mapping cache implementation.   **(06 Marks)**
    c. Explain dynamic memory allocation with its schemes.   **(06 Marks)**

4   a. What is product life cycle? Briefly explain waterfall, V cycle, spiral life cycle models.   **(10 Marks)**
    b. What are the general software design steps? Write a hardware architecture and data and counter flow diagram of a counter system and explain briefly flow diagram.   **(10 Marks)**

PART – B

5   a. What is a thread? Explain the different types of threads used in operating system.   **(06 Marks)**
    b. Describe:
        (i)   Reentrant/Non Reentrant code.
        (ii)   Foreground / Back ground system.
        (iii) Pre-emptive scheduling.   **(06 Marks)**
    c. How the information is stored in stack frame? Also explain the different types of stacks used in the memory management.   **(08 Marks)**

6   a. Define an embedded operating system with specific functions. Also explain Kernel with the various types of services.   **(08 Marks)**
    b. Design a simple operating system Kernel with a suitable code.   **(08 Marks)**
    c. What is a Task control block? What are the major components of the TCB?   **(04 Marks)**

7   a.   What is time loading? Describe the methods by which we can perform a time loading analysis of an embedded application. Discuss the advantages and disadvantages of each.

(10 Marks)

   b.   Explain Big-O notation and Big-O arithmetic used for comparing algorithms.   **(10 Marks)**

8   a.   Write a short notes on the following:
         (i)   Performance optimization.
         (ii)   Tricks of the trade.   **(10 Marks)**

   b.   Analyse the following two types of loop and determine the number of iterations to be performed and the number of steps per iteration.
         (i)   loop 1
                int sum = 0 ;
                For (int j = 0; j < N; j++)
                Sum = Sum + j ;
         (ii)   loop 2
                int sum = 0 ;
                for (int j = 0; j < 100; j++)
                Sum = Sum + j ;   **(10 Marks)**

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Seventh Semester B.E. Degree Examination, June/July 2017

DSP Algorithms and Architecture

Time: 3 hrs.   Max. Marks:100

Note: *Answer FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1   a.   Explain the major architectural features of programmable Digital Signal Processing devices. **(08 Marks)**

    b.   With the help of block diagram explain the digital filter. **(04 Marks)**

    c.   An FIR filter is described by differential equation. $y(n) = 0.6\,x(n) + 0.6\,x(n-1)$. Determine system function, frequency response, impulse response, magnitude response function and phase response. **(08 Marks)**

2   a.   Draw the structure of 4×4 Braun multiplier and explain its operation. **(08 Marks)**

    b.   Describe the implementation of single MAC unit for an 8-tap (coefficient) FIR filter. **(08 Marks)**

    c.   Find the total time required to compute the sum of 250 products using pipelined MAC unit. The MAC unit execution time is 100 nsec. **(04 Marks)**

3   a.   What is meant by addressing mode? Explain absolute, accumulator and direct addressing modes of TMS 320C54×× processor. **(08 Marks)**

    b.   Describe the operations of the following :
      i)   MPY *AR2 - , * AR4 + O, B
      ii)   MAC * AR3 - , * AR4 +, B, A
      iii)   MAS * AR3 -, * AR4 + B, A   **(06 Marks)**

    c.   Explain the hardware timer of TMS 320 C54×× DSP with logical block diagram. **(06 Marks)**

4   a.   What are the different types of serial I/O ports in C54××? Explain the application of each serial I/O port. **(08 Marks)**

    b.   With a neat diagram, describe the different stages of pipelining in C54×× processors. **(08 Marks)**

    c.   Write a TMS 320C54 ×× ALP o find a sum of a set of 4 numbers stored in on array labeled 'num'. **(04 Marks)**

PART – B

5   a.   What is the significance of Q-notation in DSP? **(04 Marks)**

    b.   Explain the IVth order FIR filter implementation with the organization of samples and filter coefficients in circular buffer. **(10 Marks)**

    c.   What is interpolation? Explain the interpolation process to implement interpolation filter with interpolation factor 'L'. **(06 Marks)**

6   a. Determine the following for 128 point FFT computation.
        i)   Number of stages
        ii) Number of butterflies in each stags
        iii) Number of butterflies needed for the entire computation
        iv) Number of butterflies that need on multiplication.   **(04 Marks)**
    b. Explain how the bit reversed index generation can be done in an 8-point DFT computation.
                                                                          (06 Marks)
    c. What is the need for scaling of inputs? Derive the scaling required in FFT calculation.
                                                                          (10 Marks)

7   a. Design a data memory system with the address range 000800h – 000FFFh for a C5416
       processor. Use 2K×8 SRAM memory chips.   **(10 Marks)**
    b. What are the features of DMA in C54×× processor?   **(04 Marks)**
    c. Explain register sub-addressing technique for configuring DMA.   **(06 Marks)**

8   a. With a neat block diagram, explain the synchronous serial interface (SSI) between C54××
       and CODEC device.   **(10 Marks)**
    b. With a neat block diagram, explain the DSP based biotelemetry receiver system.   **(10 Marks)**

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Seventh Semester B.E. Degree Examination, June/July 2017
Real Time Systems

Time: 3 hrs.　　　　　　　　　　　　　　　　　　　　　　Max. Marks:100

**Note: *Answer any FIVE full questions, selecting
atleast TWO questions from each part.***

PART – A

1 a. Give two definitions for real time system. **(04 Marks)**
   b. With a neat diagram, explain computer control system showing hardware and software interface. **(08 Marks)**
   c. Explain with block diagram sampled feedback control system. **(08 Marks)**

2 a. Explain continuous processing and laboratory system. **(08 Marks)**
   b. Draw and explain Direct Digital Control (DDC) **(08 Marks)**
   c. What are advantages of DDC over analog control? **(04 Marks)**

3 a. Explain functions of ISR with the help of flow chart. **(08 Marks)**
   b. Explain SIMD and MISD with neat diagram. **(08 Marks)**
   c. Mention features of specialized processors. **(04 Marks)**

4 a. Define CUTLASS. What are the major requirements of CUTLASS? Describe CUTLASS host target configuration. **(10 Marks)**
   b. What are the basic language requirements for RTS language along with basic language features? **(10 Marks)**

PART – B

5 a. Explain with neat diagram structure of RTOS. **(08 Marks)**
   b. Draw and explain task state diagram. **(08 Marks)**
   c. Explain cyclic and preemptive scheduling strategies. **(04 Marks)**

6 a. Explain detailed arrangement of IOSS. **(08 Marks)**
   b. Explain serially reusable code and re-entrant code. **(08 Marks)**
   c. Write a note on Liveness of RTS. **(04 Marks)**

7 a. Write a sample program to transfer of controller parameters using semaphores. **(10 Marks)**
   b. Explain with the help of flowchart mutual exclusion using conditional flags. **(10 Marks)**

8 a. Explain the outline of abstract modeling approach of ward and Mellor. **(08 Marks)**
   b. Explain software modeling with neat diagram. **(08 Marks)**
   c. Compare Ward and Mellor with Hatley and Pirbhai. **(04 Marks)**

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